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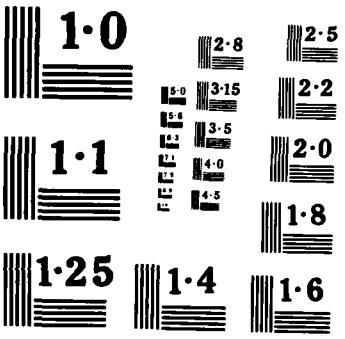

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ELECTRICAL CHARACTERISTICS OF Si DEVICES FABRICATED WITH COMPLETELY CONSUMED CARBIDE (C^3) DIELECTRIC ISOLATION PROCESS

W.-J. Lu*, A. J. Steckl* and T. P. Chow+

*Center for Integrated Electronics
Rensselaer Polytechnic Institute
Troy, New York 12181

+General Electric Company
Corporate Research and Development
Schenectady, New York 12301

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ABSTRACT

Electrical characteristics of Si devices fabricated with the C^3 dielectric isolation process have been investigated. The C^3 process produces local field oxide regions due to the differential oxidation rate of SiC versus Si (typically ~ 2-11). Si devices with good electrical properties result when the local oxidation process is allowed to Completely Consume the Carbide (C^3) film. This new process is compared to the standard silicon nitride LOCOS process. The bird's beak profiles and the damage on the Si surface resulting from both processes were investigated by SEM and Secco etch, respectively. In order to evaluate the C^3 process, MOS capacitors and Schottky barrier diodes have

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been fabricated with both techniques for varying pad oxide thickness. The measured electrical properties of these devices include lifetime, breakdown voltage, and I-V characteristics. For the minimum bird's beak case (no pad oxide), the C^3 process results in superior electrical properties over the standard nitride process.

I. Introduction

The LOCOS technology [1] for dielectric isolation is being widely used in the fabrication of VLSI circuits. In LOCOS, patterned Si_3N_4 serves as an oxidation barrier and results in local regions of thick, electrically isolating oxide. To prevent damage from occuring at the Si surface during the long thick oxide growth, a thin SiO_2 pad is required underneath the Si_3N_4 region. However, the presence of this SiO_2 pad results in lateral oxide growth, the so-called "bird's beak" [2, 3] phenomenon, which can significantly limit packing density. In a previous paper [4], we have reported on a process using SiC to produce an alternative dielectric isolation technology. The oxidation of SiC thin films has been investigated [5, 6] and found to be considerably slower than that of Si. By Completely Consuming the Carbide layer during field oxidation, the so-called C^3 process, a structure fabricated without pad oxide was obtained which is relatively free of damage and bird's beak.

In this paper, we report on the electrical characteristics of two types of devices, MOS capacitors and Schottky diodes, fabricated with the C^3 process. The properties of these devices are also compared to similar structures fabricated with the conventional LOCOS process.

II. Experimental Procedure

In order to evaluate the resulting electrical properties

of devices fabricated with a carbide-based dielectric isolation process, two types of structures were used: MOS capacitors and Schottky barrier diodes, both with aluminum electrodes. Figure 1 indicates the process flow for both the carbide - and nitride - based processes. A more detailed process has been described elsewhere [4]. 8-15 Ω-cm p-type Si wafers were used for MOS capacitors, while 3-5 Ω-cm n-type Si wafers were used for Schottky diodes. The structures with and without a thin (100 Å and 200 Å) pad oxide were fabricated and compared. The typical film thickness of SiC or Si_3N_4 is around 900 Å. All carbide films needed to be annealed in H_2 at 1100°C after deposition in order to improve their oxidation resistance. While the nitride films do not normally require to be annealed after deposition, this step was included for some of the samples in order to have a meaningful comparison with the corresponding carbide samples. Following the patterning of the carbide or nitride layer in CF_4 plasmas, field oxidation was performed in wet O_2 at 950°C for 8 hr., resulting in a field oxide thickness of 8500 Å. Under this oxidation condition, the carbide film was completely consumed, hence the C^3 process, and resulted in a 4000 Å SiO_2 layer. For the C^3 process, this oxide is etched back in HF leaving a field oxide of 4500 Å.

To fabricate the MOS capacitors, the following additional process steps were used: 500 Å gate oxide, Al deposition and patterning, backside metallization and sintering at 450°C in forming gas.

For the Schottky diodes, a similar process was used, except that no gate oxidation and no Al sintering were used. In addition, the backside of the Schottky diode samples was implanted with phosphorus followed by Al evaporation to provide ohmic contact to the Si substrate.

In the following section, the electrical properties of devices fabricated with these techniques are reported.

III. Electrical Properties

Electrical properties of the MOS capacitors and Schottky barrier diodes implemented with both C^3 and conventional LOCOS processes were measured.

(a) MOS Capacitors

For the MOS capacitors, C-V profiles and C-t measurements were performed to obtain threshold voltage, minority carrier lifetime, surface recombination velocity and other parameters. Figure 2 shows a typical C-V plot of an MOS capacitor fabricated with the C^3 process (without pad oxide). Curve (1) is the forward scan from negative to positive bias under dark conditions while curve (2) is the reverse scan. No hystersis in the C-V curve can be observed indicating a well-behaved SiO_2-Si interface. The MOS capacitor threshold voltage obtained from the C-V measurements did not vary greatly (-0.4 to -0.8V) between the two processes or as a function of pad oxide. The only samples which exhibited abnormal C-V curves were the annealed nitride structures, due to their low breakdown voltage

C-t measurements were used to determine the minority carrier generation lifetime by observing the rate at which the inversion layer forms under the MOS capacitor. Lifetime values were obtained using Heiman's method [7] and surface recombination velocities were obtained from Zerbst plots [8, 9]. Figure 3 a, b, c shows typical C-t relaxation time, Heiman's lifetime and the Zerbst plot for a C^3 sample with no pad oxide. Figure 4 a, b, c shows the corresponding parameters for a typical conventional nitride process, also with no pad oxide. Even though the nitride samples of Figure 4 were not annealed (in contrast to the C^3 samples), the lifetime is considerably lower and the surface recombination velocity is much higher.

In the case of no pad oxide, the generation lifetime of the C^3-processes samples averaged 0.9μs (over 20 samples) with a range from 0.04 to 4.2μs. For the corresponding nitride case, the average lifetime (over 17 samples) was found to be 0.07μs with a range from 0.026 to 0.13μs. Similarly, a better Si/SiO_2 interface for C^3 samples was obtained from the surface recombination velocity measurements, as determined from the Zerbst analysis. Specifically, the average S_o was 36 cm/s for the C^3 samples, as compared to an average of 91 cm/s for the conventional nitride process. Surprisingly, from the C-t data the surface properties of the C^3 samples did not seem to improve with the introduction of pad oxides as thick as 200 Å. When the nitride samples are subjected to the same annealing cycle as the carbide samples,

electrical breakdown of the device cause a very leaky C-V curve and prevents an accurate measurement of the lifetime, with and without pad oxide.

The oxide breakdown voltage is another important electrical parameter to evaluate the oxide quality resulting from the C^3 process. Figure 5 shows a matrix of breakdown field histograms for both processes. The breakdown voltage was taken as the value at which 1μA current was measured. Without pad oxide, the C^3 samples have a higher breakdown field (averaging 2.8 MV/cm) than the conventional nitride samples (which average 1.6 MV/cm), indicating that a higher degree of damage occurs in the conventional LOCOS process. Indeed, the average breakdown field is further reduced to 0.85 MV/cm if the nitride samples undergo the high temperature anneal cycle. The addition of pad oxide significantly improves the breakdown field for the C^3 samples and for the standard process, reaching 6.1 and 6.9 MV/cm, respectively, with a 200 Å pad oxide. Only in the case of the annealed nitride samples, does the pad oxide result in no improvement.

(b) Schottky Barrier Diodes

Aluminum barrier Schottky diodes fabricated with C^3 and conventional nitride processes were characterized in order to further comparatively examine the surface properties resulting from both processes. The forward I-V characteristics of four

different samples are shown in Figure 6a. Sample M is the control wafer on virgin silicon, sample A is a C^3 sample, and sample B and C are the nitride samples without and with the 1100°C anneal cycle. No pad oxide was used on all samples. In general, the Schottky barrier height ϕ_B and ideality factor n can be easily calculated from the experimental I-V characteristic [10]. It can be seen from Figure 6a that the C^3 sample resembles strongly that of the control sample in having a Schottky barrier height of 0.69 eV and an ideality factor of 1.1, similar to those reported in the literature [11]. On the other hand, the nitride samples show poorer I-V characteristics even without the high-temperature anneal, indicating a higher degree of surface damage. The nitride samples degrade further after the anneal cycle. In the case of reverse I-V characteristics, as shown in Figure 6b, the same trend applies - with control and C^3 samples having the lowest leakage and the nitride sample after anneal having the highest.

Figure 7 also shows the I-V characteristics of Schottky diodes of different samples but with 100 Å pad oxide. In order to make a comparison between C^3 and the nitride/LOCOS processed devices, the current characteristics are summarized in Table I. In this table, the current values were taken at a forward bias of 0.1 V and a reverse bias of 10 V. As far as the Schottky I-V characteristics are concerned, the devices fabricated with the C^3 process clearly show better forward and reverse bias behavior

than the devices fabricated with the conventional nitride process at the same pad oxide thickness. The devices which underwent a nitride anneal exhibit much worse characteristics.

IV. Surface Damage and Bird's Beak Profiles

In addition to the electrical study of devices fabricated by the C^3 and LOCOS processes, the damage on the Si surface from both processes was physically investigated using a Secco etch [12] to decorate defects. The Secco etch was performed after removing all the oxide from the Si surface. Figure 8a, b, c shows the surface morphology of the decorated Si surface for the samples fabricated without pad oxide. Two different kinds of damage were observed from C^3 and nitride processes. A uniform distribution of damage sites is observed for the C^3 samples, as shown in Figure 8a. On the other hand, a heavy distribution is observed at the periphery of the nitride mask for the conventional process, as shown in Figure 8b. This difference in damage pattern may be explained in the following way. For the C^3 sample the damage sites are probably due to the deposition method (sputtering) used, in that Ar incorporated in the film during deposition can subsequently result in voids. For the nitride sample, the clustering of the damage at the edge of the nitride mask (shown at higher magnification in Fig. 8c) is probably due to the very low oxidation rate of the nitride and the consequently high stress present at the mask

edge. Occasional damage sites are also seen within the mask region for the nitride sample. In the presence of pad oxide, both samples show less damage from the Secco etch. These results are consistent with the previously shown electrical characteristics of MOS capacitors and Schottky diodes.

The bird's beak profiles resulting from both C^3 and nitride LOCOS processes were investigated by SEM and are shown in Figure 9 for comparison. In the conventional nitride process, a sample with 200 Å pad oxide (Figure 9b) shows much larger bird's beak than that without pad oxide (Figure 9a). Both samples also had 500 Å gate oxide in the active region. Figure 9c and d shows the structures from the C^3 process without pad oxide. After field oxidation, the thick field oxide region and the completely consumed carbide region are clearly shown in the SEM picture (Figure 9c). The bird's beak profile after the C^3 oxide has been etched off is shown in Figure 9d.

The final bird's beak profiles resulting from the C^3 process without and with pad oxide (200 Å) are shown in Figures 9e and 9f, respectively. Both had 500 Å gate oxide on the active region.

V. Summary

The devices fabricated with the C^3 dielectric isolation process have been characterized. We have shown that the C^3 process results in superior surface properties compared to the conventional LOCOS process in the absence of pad oxide. In the MOS and

Schottky diodes measurements, an improvement in lifetime, breakdown field, and forward and reverse Schottky characteristics have been measured. In the case of no pad oxide, the MOS structures fabricated with the C^3 process yield a breakdown voltage 75% higher than those fabricated with LOCOS technology, while Schottky barrier diodes show leakage currents over 40 times smaller.

Comparing the device characteristics between a more conventional LOCOS process (with 100 Å pad oxide) and the most aggressive C^3 process (with no pad oxide), C^3 processes devices results in breakdwon voltage which is 60% lower than for LOCOS, but a Schottky barrier reverse bias leakage current which is 12 times better. From a damage study using Secco etch for both C^3 and LOCOS process, it was found that without pad oxide the C^3 samples are superior in having more uniform and possibly lower damage distribution as shown in the SEM photographs. The structures resulting from the C^3 process also show a moderate and well-behaved bird's beak effect. In conclusion, it appears that the C^3 process is a promising technique for dielectric isolation of integrated circuits.

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LIST OF FIGURES

FIGURES (con't)

(d) C^3 process without pad oxide (after etching back oxide)

(e) C^3 process without pad oxide; 500Å gate oxide

(f) C^3 process with 200 Å pad oxide; 500 Å gate oxide.

LIST OF TABLE

TABLE I

PAD OXIDE / Process	Reverse bias at 10V (10^{-6} A)		Forward Bias at 0.1V (10^{-6} A)	
	0	100 Å	0	100 Å
C^3	1	2	0.5	0.6
LOCOS	42	12	4.5	5.5
Nitride Anneal	$>10^4$	30	$1.5x10^3$	13

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